Homework 1

(Due date: January 18th @ 5:30 pm)
Presentation and clarity are very important!

PROBLEM 1 (27 PTS)

a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (14 pts)

- ✓ $F=\overline{Y(Z+\bar{X})+\overline{\bar{X}Y}}$
- ✓ $F=\prod(M_1,M_4,M_5,M_7)$
- ✓ $F(A,B,C)=\overline{AB\bar{C}+(\overline{A\oplus C})B}$
- ✓ $F=\overline{XY\bar{Z}+\bar{X}(\bar{Y}\oplus\bar{Z})}$

b) Demonstrate the following Theorem: (5 pts)

$$(X+Y)(\bar{X}+Z)(Y+Z)=(X+Y)(\bar{X}+Z)$$

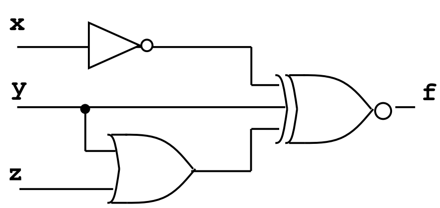
c) For the following Truth table with two outputs: (8 pts)

- Provide the Boolean functions using the Canonical Sum of Products (SOP), and Product of Sums (POS).
- Express the Boolean functions using the minterms and maxterms representations.
- Sketch the logic circuits as Canonical Sum of Products and Product of Sums.

x	y	z	f_1	f_2
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

PROBLEM 2 (26 PTS)

a) Construct the truth table describing the output of the following circuit and write the simplified Boolean equation (8 pts). Note that $a\oplus b\oplus c=(a\oplus b)\oplus c=a\oplus(b\oplus c)=b\oplus(a\oplus c)$

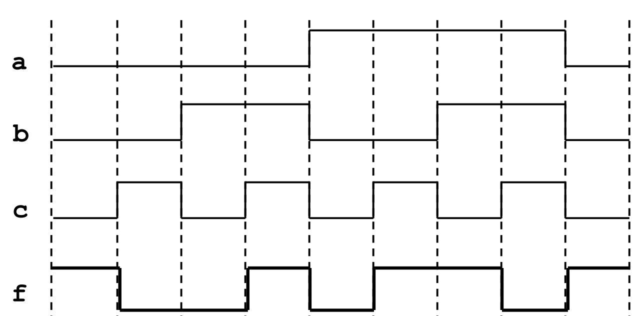


x	y	z	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

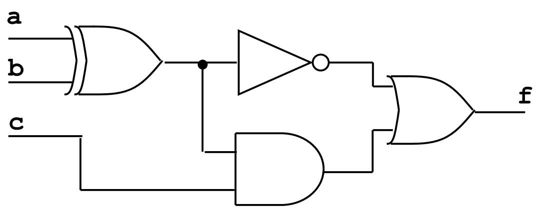
$f=$

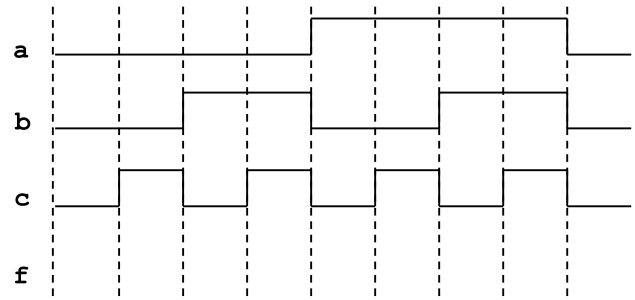
b) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (8 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
 port ( a, b, c: in std_logic;
        f: out std_logic);
end circ;

architecture st of circ is
-- ???
begin
-- ???

end st;
```



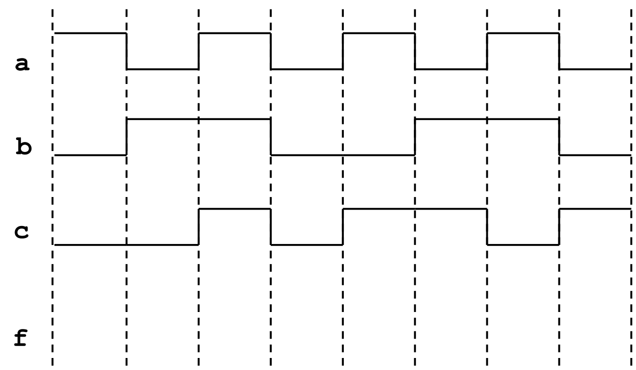
c) Complete the timing diagram of the following circuit: (5 pts)





d) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (5 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture st of circ is
  signal x, y: std_logic;

begin
  x <= a nor b;
  y <= x xor c;
  f <= y xnor (not a);
end st;
```



PROBLEM 3 (11 PTS)

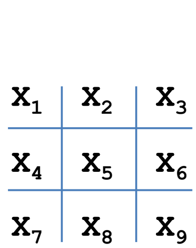
- Complete the truth table for a circuit with 4 inputs x, y, z, w that activates an output ($f = 1$) when the number of 1's in the inputs is equal than the number of 0's. For example: If $xyzw = 1001 \rightarrow f = 1$. If $xyzw = 1011 \rightarrow f = 0$.
- Provide the Boolean equation for the output f and sketch the logic circuit.

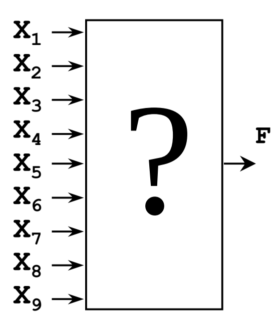
PROBLEM 4 (11 PTS)

- Tic-tac-toe game: It is played on a 3-by-3 grid of squares: The players alternate turns. Each player chooses a square and places a mark in a square (one player uses **X** and the other **O**). The first player with three marks in a row, column, or diagonal wins the game.

- A logical circuit is to be designed for an electronic tic-tac-toe that indicates the presence of a winning pattern for a player. The circuit has 9 inputs (X_1 to X_9) and an output **F**. **F** is '1' if a winning pattern is present and a 0 otherwise.

  ✓ Provide the Boolean expression for **F**. The 9 inputs (X_1 to X_9) are arranged in the following pattern:



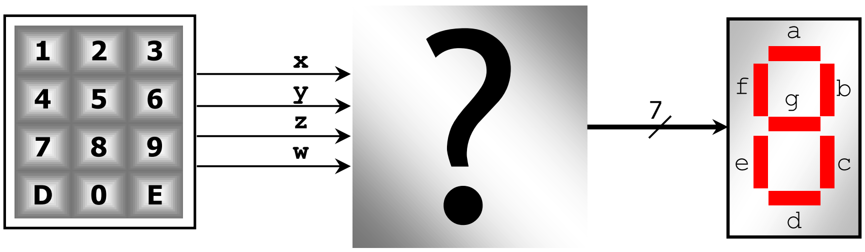


  ✓ Sketch the logical circuit resulting from the Boolean equation for **F**.

PROBLEM 5 (25 PTS)

- A numeric keypad produces a 4-bit code as shown below. We want to design a logic circuit that converts each 4-bit code to a 7-segment code, where each segment is an LED. The LEDs are lit with a logical '0' (negative logic). The inputs are active high (or in positive logic).

✓ Complete the truth table for each output (a, b, c, d, e, f, g).
✓ Provide the simplified expression for each output (a, b, c, d, e, f, g). Use Karnaugh maps for a, b, c, d, e and the Quine-McCluskey algorithm for f, g. Note that it is safe to assume that the codes `1100` to `1111` will not be produced by the keypad.



Value	X	Y	Z	W	a	b	c	d	e	f	g
0	0	0	0	0							
1	0	0	0	1							
2	0	0	1	0							
3	0	0	1	1							
4	0	1	0	0							
5	0	1	0	1							
6	0	1	1	0							
7	0	1	1	1							
8	1	0	0	0							
9	1	0	0	1	0	0	0	0	1	0	0
E	1	0	1	0							
D	1	0	1	1							
	1	1	0	0							
	1	1	0	1							
	1	1	1	0							
	1	1	1	1